WHAT IS CLAIMED IS:

1. A computer-implemented method for identifying the best process path in a semiconductor manufacturing process for processing a plurality of wafer lots, comprising:

providing a plurality of operations in the semiconductor manufacturing process;

providing a plurality of tools in at least one of the plurality of operations;

providing a plurality of process paths;

providing a plurality of lot yields corresponding to the plurality of wafer lots;

setting the plurality of lot yields as responses;

setting the plurality of operations as control factors;

setting the plurality of tools as factor levels in response to at least one of the plurality of operations;

determining at least one of the plurality of operations by using an analysis of variance method with the responses, control factors, and factor levels;

determining a best tool for the one of the plurality of operations having the most influence by retrieving a maximum statistical characteristic; and

outputting at least one best process path from the plurality of process paths, wherein the at least one best process path includes the best tool.

2. The method as claimed in claim 1, wherein the statistical characteristic comprises a signal to noise ratio.

3. The method as claimed in claim 1, wherein the statistical characteristic comprises an average yield.

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4. The method as claimed in claim 3, further comprising determining at least one of the plurality of tools corresponding to the at least one of the plurality of operations as having the most contribution to the average yield.

5. The method as claimed in claim 3, wherein the step of determining at least one of the plurality of operations by using an analysis of variance method includes,

comparing each of the plurality of operations relative to the average yield,

ignoring the plurality of operations having only a single tool, and

considering the plurality of operations having a greater than a predetermined level of contribution over the average yield.

6. The method as claimed in claim 1, wherein the best process path includes the tool having the most contribution.

7. A computer-readable medium storing instructions executable by a processor for identifying the best process path in a semiconductor manufacturing process for processing a plurality of wafer lots, comprising:

providing a plurality of operations in the semiconductor manufacturing process;

providing a plurality of tools in at least one of the plurality of operations;

providing a plurality of process paths;

providing a plurality of lot yields corresponding to the plurality of wafer lots;

setting the plurality of lot yields as responses;

setting the plurality of operations as control factors;

setting the plurality of tools as factor levels in response to at least one of the plurality of operations;

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determining at least one of the plurality of operations by using an analysis of variance method with the responses, control factors, and factor levels;

determining a best tool for the one of the plurality of operations having the most influence by retrieving a maximum statistical characteristic; and

outputting at least one best process path from the plurality of process paths, wherein the at least one best process path includes the best tool.

8. The computer-readable medium as claimed in claim 7, wherein the statistical characteristic comprises a signal to noise ratio.

9. The computer-readable medium as claimed in claim 7, wherein the statistical characteristic comprises an average yield.

10. The computer-readable medium as claimed in claim 9, further comprising determining at least one of the plurality of tools corresponding to the at least one of the plurality of operations as having the most contribution to the average yield.

11. The computer-readable medium as claimed in claim 9, wherein the step of determining at least one of the plurality of operations by using an analysis of variance method includes,

comparing each of the plurality of operations relative to the average yield,

ignoring the plurality of operations having only a single tool; and

considering the plurality of operations having a greater than a predetermined level of contribution over the average yield.

12. A computer-implemented method for identifying the best process path in a semiconductor manufacturing process, comprising:

providing a plurality of operations in the semiconductor manufacturing process;

providing a plurality of tools in at least one of the plurality of operations;

providing a plurality of process paths;

providing a plurality of lot yields corresponding to the plurality of wafer lots;

setting the plurality of lot yields as responses;

setting the plurality of operations as control factors;

setting the plurality of tools as factor levels in response to at least one of the plurality of operations;

determining at least one of the plurality of operations by using an analysis of variance method with the responses, control factors, and factor levels;

determining a best tool for the one of the plurality of operations having the most influence by retrieving a maximum statistical characteristic; and

outputting at least one best process path from the plurality of process paths, wherein the at least one best process path includes the best tool.

13. The method as claimed in claim 12, wherein the statistical characteristics is a signal to noise ratio of the plurality of wafer yields.

14. The method as claimed in claim 12, wherein the best process path of the semiconductor process includes the tool having the most contribution.

15. A system for determining best process paths in a semiconductor manufacturing process including a plurality of operations, comprising

a yield database for storing a plurality of yield data corresponding to a plurality of wafer lots manufactured by the specific manufacturing process, wherein

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each of the plurality of wafer lots includes a plurality of wafers, and wherein the plurality of yield data corresponds to the plurality of the plurality of wafer lots;

a process history database for storing a plurality of process path data;

a memory for storing a program; and

a microprocessor for performing the program, the microprocessor reading the plurality of yield data and process path data, using an analysis of variance method for identifying the most influential operation from the plurality of operations.

16. The system as claimed in claim 15, wherein the most influential operation includes a plurality of tools, and the microprocessor identifies at least one tool from the plurality of tools as being the best tool.

17. The system as claimed in claim 16, wherein a best process path of the semiconductor process includes the best tool.

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